"FORMATION OF LATTICE-TUNING SEMICONDUCTOR SUBSTRATES"

This invention relates to the production of lattice-tuning semiconductor substrates, and is more particularly, but not exclusively, concerned with the production of relaxed SiGe (silicon/germanium) "virtual substrates" suitable for the growth of strained silicon or SiGe active layers and unstrained III-V semiconductor active layers within which active semiconductor devices, such as MOSFETs, may be fabricated.

It is known to epitaxially grow a strained Si layer on a Si wafer with a relaxed SiGe buffer layer interposed therebetween, and to fabricate semiconductor devices, such as MOSFETs, within the strained Si layer in order to enhance the properties of the semiconductor devices. The buffer layer is provided in order to increase the lattice spacing relative to the lattice spacing of the underlying Si substrate, and is generally called a virtual substrate.

It is also known to epitaxially grow an alloy of silicon and germanium (SiGe) on the silicon substrate to form the buffer layer. Since the lattice spacing of SiGe is greater than the normal lattice spacing of Si, the desired increase in lattice spacing is achieved by the provision of such a buffer layer if the buffer layer is allowed to relax.

The relaxation of the buffer layer inevitably involves the production of dislocations in the buffer layer to relieve the strain. These dislocations generally form a half loop from the underlying surface which expands to form a long dislocation at the strained interface. However the production of threading dislocations which extend through the depth of the buffer layer is detrimental to the quality of the substrate, in that such dislocations can produce an uneven surface and can cause scattering of electrons within the active semiconductor devices. Furthermore, since many dislocations are required to relieve the strain in a SiGe layer, such dislocations inevitably interact with one another causing pinning of threading dislocations. Additionally more dislocations are required for further relaxation, and this can result in a higher density of threading dislocations.

Known techniques for producing such a buffer layer, such as are disclosed in US5442205, US 5221413, WO 98/00857 and JP 6-252046, involve linearly grading the Ge composition in the layer in order that the strained interfaces are distributed over the graded region. This means that the dislocations that form are also distributed over the graded region and are therefore less likely to interact. However such techniques suffer from the fact that the main sources of dislocations are multiplication mechanisms in which many dislocations are generated from the same source, and this causes the dislocations to be clustered in groups, generally on the same atomic glide planes. The strain fields from these groups of dislocations can cause the virtual substrate surface to have large undulations which is both detrimental to the quality of the virtual substrate and has the added effect of trapping threading dislocations.

US 2002/0017642A1 describes a technique in which the buffer layer is formed from a plurality of laminated layers comprising alternating layers of a graded SiGe layer having a Ge composition ratio which gradually increases from the Ge composition ratio of the material on which it is formed to an increased level, and a uniform SiGe layer on top of the graded SiGe layer having a Ge composition ratio at the increased level which is substantially constant across the layer. The provision of such alternating graded and uniform SiGe layers providing stepped variation in the Ge composition ratio across the buffer layer makes it easier for dislocations to propagate in lateral directions at the interfaces, and consequently makes it less likely that threading dislocations will occur, thus tending to provide less surface roughness. However this technique requires the provision of relatively thick, carefully graded alternating layers in order to provide satisfactory performance, and even then can still suffer performance degradation due to the build-up of threading dislocations.

It is an object of the invention to provide a method of forming a lattice-tuning semiconductor substrate in which performance is enhanced by decreasing the density of threading dislocations as compared with known techniques.

According to the present invention there is provided a method of forming a lattice-tuning semiconductor substrate, comprising:

(a)   defining a selected area (12) of a semiconductor surface (15) by means of a window (13) extending through an isolating layer (11) on the semiconductor surface (15);

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(b)   defining in the vicinity of the window (13) a depression (14) in the isolating layer (11);

(c)   growing on top of the selected area (12) of the semiconductor surface
10   (15) an active layer (16) of a semiconducting material that is not lattice-matched to the material of the semiconductor surface (15) such that dislocations (17) are formed in the window (13) to relieve the strain in the active layer (16); and

(d)   further growing the active layer (16) to overgrow the isolating layer (11)
15   and extend into the depression (14) to form a substantially dislocation-free area (18) of said semiconducting material within the depression (14).

Such a technique is capable of producing high quality virtual substrates, of SiGe for example, with extremely low levels of threading dislocations, that is with levels
20   from less than 10^6 dislocations per cm^2 to virtually no threading dislocations. This is as a result of the fact that the dislocations produced in the SiGe layer within the window prior to further growth of the SiGe layer serve to relieve the strain in the SiGe layer, so that, when the overgrowth of the SiGe layer occurs, the area of SiGe within the depression is produced substantially without dislocations. The resulting virtual
25   substrate is of superior quality. The quality of the virtual substrate produced may be such as to render it suitable for specialised applications, for example in microelectronics or in full CMOS integration systems.

This technique has particular advantage in that the virtual substrate does not
30   cover the whole of the wafer, but instead is only present in pre-defined areas. These areas may be as small as required, and may, for example, be the size of an electronic

device so that the benefits of strained silicon can be employed without affecting the processing of the other devices on the wafer.

5   In a preferred embodiment of the invention the portion of the active layer that has overgrown the isolating layer is removed after the growing of the active layer to extend into the depression, so as to isolate the substantially dislocation-free area of said semiconducting material within the depression from the area of said semiconducting material within the window.   Preferably the portion of the active layer that has overgrown the isolating layer is removed by polishing down to the level of the isolating

10   layer. Once the surface has been polished flat a substantially dislocation-free virtual substrate is left, completely isolated from the substrate by the material of the isolating layer, which will usually be a Si oxide layer.

     In a further development of the invention the active layer and the isolating layer

15   are removed from the semiconductor surface after the growing of the active layer to extend into the depression, except in the vicinity of the depression, so as to leave on the semiconductor surface the substantially dislocation-free area of said semiconducting material isolated from the semiconductor surface by the portion of the isolating layer. Preferably the active layer and the isolating layer are removed from the semiconductor

20   surface by etching.   The virtual substrate left on the oxide would then be an ideal template for strained silicon devices which could be integrated with "normal" silicon devices on the semiconductor substrate. The virtual substrate need therefore only be fabricated underneath devices which need the performance enhancements of strained silicon. The oxide underneath the virtual substrate would usually be arranged to be thin

25   in order that the surface is kept as planar as possible for device processing.

     The active layer may be annealed at an elevated temperature in order to substantially fully relieve the strain in the active layer. Furthermore the growth of the active layer may be carried out at a temperature in the range from room temperature to

30   1200°C, and preferably in the range from 350 to 900°C, and the annealing of the active layer may be carried out at an elevated temperature in the range from room temperature to 1500°C, and preferably in the range from 500 to 1200°C.

The active layer may have a Ge composition ratio that is substantially constant within the active layer. Alternatively the active layer may comprise first and second sub-layers, one of the sub-layers having a Ge composition ratio that is substantially constant within the sub-layer, and the other sub-layer having a Ge composition ratio that increases within the layer from a first level to a second level greater than the first level. In this case intermediate processing may be conducted between the growth of the first and second sub-layers. The intermediate processing may incorporate a step of annealing the first sub-layer at an elevated temperature in order to substantially fully relieve the strain in the first sub-layer. Furthermore the intermediate processing step may incorporate a chemo-mechanical polishing step.

The active layer may be grown by a selective epitaxial growth process, such as chemical vapour deposition (CVD).

In order that the invention may be more fully understood, reference will now be made to the accompanying drawings, in which:

Figures 1 to 5 are explanatory cross-sectional views showing successive steps in the formation of a lattice-tuning semiconductor substrate in accordance with the invention.

The following description is directed to the formation of a virtual lattice-tuning Si substrate on an underlying Si substrate with the interposition of a SiGe buffer layer. However it should be appreciated that the invention is also applicable to the production of other types of lattice-tuning semiconductor substrates, including substrates terminating at fully relaxed pure Ge allowing III-V incorporation with silicon. It is also possible in accordance with the invention to incorporate one or more surfactants, such as antimony for example, in the epitaxial growth process in order to produce even smoother virtual substrate surfaces and lower density threading dislocations by reducing surface energy.

Referring to Figure 1, in the exemplary method in accordance with the invention for forming a relaxed SiGe virtual substrate suitable for growth of strained Si or SiGe active layers and unstrained III-V semiconductor active layers within which active semiconductor devices, such as MOSFETs, may be fabricated, an isolating layer 11 of

5   Si oxide is grown on a Si substrate 10 and is then selectively etched after the area to be etched has been defined, for example by the application of a photoresist layer to the oxide layer and the selective exposure and development of the photoresist layer to form a photoresist mask. This etching step produces at least one window 13 extending all the way through the oxide to the Si surface 15 and at least one depression 14 extending only

10 part of the way through the oxide so as to be separated from the Si surface 15 by an underlying portion of the oxide layer 11. The different etching depths of the windows 13 and depressions 14 are produced in known manner, for example by two separate masking and etching steps applied sequentially. For example, the isolating layer 11 could consist of a two separate isolating films on top of each other, such as a silicon

15 nitride film on top of a silicon oxide film. To produce the depressions 14, a mask and photoresist could be used to expose the areas to be etched and selective etching of the upper isolating film could then be achieved using selective chemical etches or reactive ion etches, with the lower isolating film acting as an etch-stop. The window 13 could than be produced using a further mask and photoresist to expose the area to be etched,

20 and using an etch to etch through both the upper isolating film and the lower isolating film.

Referring to Figure 2, in a subsequent selective CVD epitaxial growth process, a SiGe layer 16 is grown on the selected area 12 of the Si surface 15 defined by

25 the window 13 through the oxide layer 11 at a temperature in the range from room temperature to 1200°C, and preferably in the range from 350 to 900°C. This is possible with the addition of HCl into the growth gases or chlorinated precursors (e.g. dichloro-silane) that produce HCl during growth such that the HCl effectively "etches" any polycrystalline growth that occurs on the oxide, whilst leaving the crystalline growth in

30 the windows intact. This occurs because the weak bonding of the polysilicon layer to the oxide allows the HCl to easily etch any deposition, whereas the strong bonding of the silicon (or germanium) to the silicon of the substrate is impervious to the HCl. As

this SiGe layer 16 is grown the strain is eventually relaxed by the formation of dislocations 17 within SiGe layer 16. These dislocations 17 generally extend from the boundaries between the SiGe layer 16 and the surrounding oxide layer 11 to the upper surface of the SiGe layer 16.

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When the SiGe growth reaches the top of the oxide layer 11, it overgrows laterally onto the oxide layer 11 as a single crystal, as shown in Figure 3. This process is known as epitaxial lateral overgrowth (ELO) and is used to fill each depression 14 in the oxide layer 11 close to the window 13. Because of the mechanics of the dislocations 10 17 that have formed in the window 13 to relieve the strain in the SiGe layer 16, substantially no dislocations are formed in the ELO filled depressions 14. This is because the dislocations 17 are only produced at the interface of a mismatched layer, that is in this case at the interface between the substrate 10 and the SiGe layer 16, which only occurs in the window 13. Since the dislocations 17 are confined to their glide 15 planes which are at an angle to the Si surface 15, all the dislocations 17 rise from the oxide window 13 at an angle. The dislocations 17 cannot reach parts of the crystal away from the window 13, and, since there is no lattice mismatch, no further dislocations will form in the depressions 14 leaving SiGe crystal material substantially free from defects within the depressions 14.

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If required the relaxation of the SiGe layer may be assisted by an annealing step carried out at an elevated temperature in the range from room temperature to 1500°C, and preferably in the range from 500 to 1,200°C, possibly with epitaxial growth of SiGe material continuing after this annealing step at a temperature in the range from room 25 temperature to 1200°C, and preferably in the range from 350 to 900°C, to form a further SiGe layer continuous with the first SiGe layer until lateral overgrowth of the SiGe material onto the top of the oxide layer 11 occurs.

After filling of the depressions 14 with Si Ge the surface of the wafer is polished 30 flat down to the level of the oxide layer 11 in order to remove those parts of the SiGe layer 16 that have overgrown the oxide layer 11, thereby leaving substantially dislocation-free virtual substrates 18 of Si Ge completely isolated from the underlying

substrate 10 and from the SiGe within the window 13 by the surrounding oxide, as shown in Figure 4.

Referring to Figure 5, it is possible in a further optional step to etch all the oxide
5   and epitaxy away except for the virtual substrate 18 on the underlying oxide. This can be done by a selective etching step after the area to be etched has been defined, for example by the application of a photoresist layer and the selective exposure and development of the photoresist layer to form a photoresist mask. This would then be an ideal template for strained silicon devices which could be integrated with "normal"
10 silicon devices on the silicon substrate. The virtual substrate need only be fabricated underneath the devices which need the performance enhancements of strained silicon. In this case the oxide underneath the virtual substrates would need to be thin in order that the surface is kept as planar as possible for device processing.

15 In this manner a high quality virtual substrate is produced which may be used for the growth of strained Si or SiGe active layers and unstrained III-V semiconductor active layers within which active semiconductor devices may be fabricated.

The Ge composition within the SiGe material may be substantially constant
20 through the thickness of the SiGe layer 16, although it would also be possible for the Ge composition to be graded so that it increases from a first composition at a lower level in the layer to a second, higher composition at a higher level in the layer.

Various modifications of the above-described method are possible within the
25 scope of the invention. For example, instead of the depressions being separated from the window by intervening parts of the isolating layer, the depressions could be formed by stepped edges at the sides of the window, so that the lateral overgrowth of the Si Ge layer onto the step forms the virtual substrate. This essentially amounts to the depressions overlapping the window, and prevent the need for the overgrowth to grown
30 down into the depressions.

Furthermore a similar method may be used for growth of any appropriate semiconductor material other than SiGe on to a substrate with which it has a lattice mismatch. The same dislocation dynamics would apply as described above in the production of a substantially defect-free virtual substrate of such other materials. Examples of suitable other materials that could be grown in this manner include SiC, SiGeC, InP and GaAs. In the case of the growth of GaAs onto silicon, which is advantageous in the field of optoelectronics, the GaAs is grown directly on the Si substrate without the need for a separate virtual substrate.

This fabrication technique may be used to produce a virtual substrate in only one or more selected areas of the chip (as may be required for system-on-a-chip integration) in which enhanced circuit functionality is required, for example.

The method of the invention is capable of a wide range of applications, including the provision of a virtual substrate for the growth of strained or relaxed Si, Ge or SiGe layers for fabrication of devices such as bipolar junction transistors (BJT), field effect transistors (FET) and resonance tunnelling diodes (RTD), as well as III-V semiconductor layers for high speed digital interface to CMOS technologies and optoelectronic applications including light emitting diodes (LEDs) and semiconductor lasers.